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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,468	09/23/2003	Yong Zhang	50T5646.01	2940

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EXAMINER	
MALEK, LEILA	
ART UNIT	PAPER NUMBER
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/29/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/668,468	ZHANG, YONG	
	Examiner	Art Unit	
	Leila Malek	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 11-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 11-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *09/23/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement submitted on 09/23/2003 has been considered and made of record by the examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ebuchi et al. (hereafter, referred as Ebuchi) (US 2001/0030565), in view of Boerstler (US 2002/0172312).

As to claim 1, Ebuchi discloses a multi-phase clock generator (see the abstract and paragraph 0001) for receiving a clock signal (i.e. the reference clock signal RFECLK) defining a clock pulse period (see paragraph 0051 wherein the frequency of the clock signal has been determined); using the clock signal, generating at least one correction clock pulse (see paragraph 0051 and Fig. 3), the correction clock pulse being temporally within a single clock period (see Fig. 4 and paragraph 0051, i.e. since T(period)=1/f(frequency); and frequency of the reference clock signal is 25MHZ and frequency of each of the clock signals is 100 MHZ, therefore the correction clock pulse is within a single clock period). Ebuchi discloses all the subject matters claimed in claim 1, except for using at least one correction clock pulse and latching values in

plural data streams. Boerstler, in the same field of endeavor, discloses a system and method for reducing timing uncertainties in a serial data signal (see the abstract). Boerstler discloses a retiming mechanism 205, which has been configured to receive serial data 201 (interpreted as plural data streams) transmitted from the transmitter 101. Boerstler further discloses that retiming mechanism in receiver 103 may further be configured to receive phase of clock generated from an oscillator 204 and select a particular phase of the clock generated by oscillator 204 to sample serial data 201 during a period of serial data 201 to reduce timing uncertainties, i.e., jitter, in the serial data (See paragraph 0060). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Ebuchi as suggested by Boerstler to sample the data with one of the clocks for the reasons stated above.

As to claim 2, Ebuchi discloses generating at least 2N correction clock pulses for a single clock period, wherein N is an integer (see Fig. 3 and paragraph 0051).

3. Claims 3, 7, and 8, are rejected under 35 U.S.C. 103(a) as being unpatentable over Ebuchi, and Boerstler, further in view of Wang et al. (US 7,020,227).

As to claim 3, Boerstler further discloses that at least two data streams have respective bits defining a temporally overlapping time period (see Fig. 3, jitter), Ebuchi and Boerstler disclose all the subject matters claimed in claim 3, except that method includes using at least one correction clock pulse in the overlapping time period to latch values in the streams. However, Boerstler discloses that jitter may be diminished by sampling the serial data signal 201 at a point in time when the serial data signal 201 is not likely to experience jitter (see paragraphs 0030 and 0060). It is well known in the

art that if the data streams have been received in parallel instead of serial the parts of the data stream that overlap with each other are the jitter free parts (i.e. it means that they do not have any phase offset compare to each other). Therefore, based on Boerstler's teaching it would have been obvious to one of ordinary skill in the art at the time of invention to use at least one correction clock pulse in the overlapping time period (i.e. the jitter free time period) to sample the data stream in order to diminish the jitter in the system (see paragraph 0030). Also it would have been obvious to one of ordinary skill in the art at the time of invention to send data streams in parallel instead of serial to reduce the required processing speed of the phase detector (e.g. as evidence by Wang, see column 1, paragraph 4).

As to claim 7, Ebuchi discloses a multi-phase clock generator (see the abstract and paragraph 0001) for receiving a clock signal (i.e. the reference clock signal RFECLK) defining a clock pulse period (see paragraph 0051 wherein the frequency of the clock signal has been determined); using the clock signal, generating at least one correction clock pulse (see paragraph 0051 and Fig. 3), wherein the correction clock signal having a frequency higher than the clock pulse frequency (i.e. 100 MHZ compare to 25 MHZ). Ebuchi discloses all the subject matters claimed in claim 7, except for using at least one correction clock pulse within an overlapping period defined by the at least two bits and latching values of at least two bits in respective data streams. Boerstler, in the same field of endeavor, discloses a system and method for reducing timing uncertainties in a serial data signal (see the abstract). Boerstler discloses a retiming mechanism 205, which has been configured to receive serial data

201 (interpreted as plural data streams) transmitted from the transmitter 101. Boerstler further discloses that retiming mechanism in receiver 103 may further be configured to receive phase of clock generated from an oscillator 204 and select a particular phase of the clock generated by oscillator 204 to sample serial data 201 during a period of serial data 201 to reduce timing uncer0tainties, i.e., jitter, in the serial data (see paragraph 0060). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Ebuchi as suggested by Boerstler to sample the data with one of the clocks for the reasons stated above. Boerstler further discloses that at least two data streams have respective bits defining a temporally overlapping time period (see Fig. 3, jitter), Ebuchi and Boerstler disclose all the subject matters claimed in claim 7, except that the method includes using at least one correction clock pulse in the overlapping time period to latch values in the streams. However, Boerstler discloses that jitter may be diminished by sampling the serial data signal 201 at a point in time when the serial data signal 201 is not likely to experience jitter (see paragraph 0030). It is well known in the art that if the data streams have been received in parallel instead of serial, the parts of the data streams that overlap with each other are the jitter free parts (i.e. it means that they do not have any phase offset compare to each other). Therefore, based on Boerstler's teaching it would have been obvious to one of ordinary skill in the art at the time of invention to use at least one correction clock pulse in the overlapping time period (i.e. the jitter free time period) to sample the data stream in order to diminish the jitter in the system (see paragraph 0030). Also it would have been obvious to one of ordinary skill in the art at the time of invention to send data streams

in parallel instead of serial to reduce the required processing speed of the phase detector (e.g. as evidence by Wang, see column 1, paragraph 4).

As to claim 8, Ebuchi discloses that the correction clock module generates at least 2N correction clock pulses for a single clock signal period, wherein N is an integer (see Fig. 3 and paragraph 0051).

4. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ebuchi and Boerstler, further in view of Tang et al. (hereafter, referred as Tang) (US 2002/0056854).

As to claim 4, Ebuchi and Boerstler disclose all the subject matters claimed in claim 1, except that the clock signal is received from a phase locked loop. Tang, in the same field of endeavor, discloses a DLL (Delay Locked Loop) and PLL (Phase Locked Loop), which are used to align a particular signal with the same frequency and phase of a reference clock signal (see paragraph 0003). Tang further discloses that the clock and data recovery circuit 350 includes a PLL for generating a periodic input (interpreted as the reference clock signal) to feed into a DLL (see paragraph 0019). It would have been obvious to one of ordinary skill in the art at the time of invention modify Ebuchi and Boerstler as suggested by Tang to improve the clock and data recovery process (see paragraphs 0008, 0009, and 0020).

As to claim 5, Ebuchi further disclose feeding back an output of the VCO to a phase detector receiving the clock signal (see Fig. 3).

As to claim 6, Ebuchi and Boerstler disclose all the subject matters claimed in claim 1, except that selecting at least on correction clock pulse has been performed by

using at least one selector element and at least one de-multiplexer. Tang discloses a phase selector 501 (see Fig. 2 and paragraphs 0021-0023), comprising a control logic circuit (interpreted as the selector) and a selector (interpreted as the de-multiplexer). It would have been obvious to one of ordinary skill in the art at the time of invention modify Ebuchi and Boerstler as suggested by Tang to improve the clock and data recovery process (see paragraphs 0008, 0009, and 0020).

5. Claims 9, 11, 12, are rejected under 35 U.S.C. 103(a) as being unpatentable over Ebuchi, Boerstler, and Wang, further in view of Tang.

As to claim 9, Ebuchi, Boerstler, and Wang disclose all the subject matters claimed in claim 7, except that the clock signal is received from a phase locked loop. Tang, in the same field of endeavor, discloses a DLL (Delay Locked Loop) and PLL (Phase Locked Loop), which are used to align a particular signal with the same frequency and phase of a reference clock signal (see paragraph 0003). Tang further discloses that the clock and data recovery circuit 350 includes a PLL for generating a periodic input (interpreted as the reference clock signal) to feed into a DLL. It would have been obvious to one of ordinary skill in the art at the time of invention modify Ebuchi, Boerstler, and Wang as suggested by Tang to improve the clock and data recovery process (see paragraphs 0008, 0009, and 0020).

As to claim 11, Ebuchi discloses that an output of the VCO is fed back to a phase detector receiving the clock signal (see Fig. 3).

As to claim 12, Ebuchi, Boerstler, and Wang disclose all the subject matters claimed in claim 11, except that selecting at least one correction clock pulse has been

performed by using at least one selector element and at least one de-multiplexer. Tang discloses a phase selector 501 (see Fig. 2 and paragraphs 0021-0023), comprising a control logic circuit (interpreted as the selector) and a selector (interpreted as the de-multiplexer). It would have been obvious to one of ordinary skill in the art at the time of invention modify Ebuchi and Boerstler as suggested by Tang to improve the clock and data recovery process (see paragraphs 0008, 0009, and 0020).

6. Claims 13, 14, and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boerstler, in view of Wang.

As to claim 13, Boerstler discloses a jitter correction system (see the abstract) comprising: means for generating plural correction clock pulses for each clock pulse of a clock signal (See Fig. 9, block 902); Boerstler discloses all the subject matters claimed in claim 13, except means for correlating at least a first correction clock pulse with at least two data bits received in respective parallel data streams; and means for identifying values of the data bits at least in part using the first correction clock pulse. However, Boerstler discloses that jitter may be diminished by sampling the serial data signal 201 at a point in time when the serial data signal 201 is not likely to experience jitter (see paragraph 0030). It is well known in the art that if the data streams have been received in parallel instead of serial, the parts of the data streams that overlap with each other are the jitter free parts (i.e. it means that they do not have any phase offset compare to each other). Therefore, based on Boerstler's teaching it would have been obvious to one of ordinary skill in the art at the time of invention to use at least one correction clock pulse (i.e. interpreted as correlating at least a first correction clock

pulse with at least two data bits received in respective parallel data streams) in the overlapping time period (i.e. the jitter free time period) to sample (interpreted as identifying values of the data bits at least in part using the first correction clock pulse) the data stream in order to diminish the jitter in the system (see paragraph 0030). Also it would have been obvious to one of ordinary skill in the art at the time of invention to send data streams in parallel instead of serial to reduce the required processing speed of the phase detector (e.g. as evidence by Wang et al. (US 7,020,227), see column 1, paragraph 4).

As to claim 14, Boerstler further discloses that means for generating includes at least one voltage controlled oscillator (VCO) (paragraphs 0025 and 0035).

As to claim 16, Boerstler discloses generating at least 2N correction clock pulses for a single clock period, wherein N is an integer (see paragraph 0028).

As to claim 17, Boerstler discloses that jitter may be diminished by sampling the serial data signal 201 at a point in time when the serial data signal 201 is not likely to experience jitter (See paragraph 0030). It is well known in the art that if the data streams have been received in parallel instead of serial, parts of the data streams that overlap with each other are the jitter free parts (i.e. it means that they do not have any phase offset compare to each other). Therefore, based on Boerstler's teaching it would have been obvious to one of ordinary skill in the art at the time of invention to use at least one correction clock pulse (i.e. interpreted as correlating at least a first correction clock pulse with at least two data bits received in respective parallel data streams) in the overlapping time period (i.e. the jitter free time period) to sample (interpreted as

identifying values of the data bits at least in part using the first correction clock pulse) the data stream in order to diminish the jitter in the system (see paragraph 0030). Also it would have been obvious to one of ordinary skill in the art at the time of invention to send data streams in parallel instead of serial to reduce the required processing speed of the phase detector (for instance as evidence by Wang, see column 1, paragraph 4).

As to claim 18, Boerstler further disclose feeding back an output of the VCO to a phase detector receiving the clock signal (see Fig. 2).

7. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Boerstler and Wang, further in view of Applicant's admitted prior art (background of invention).

As to claim 15, Boerstler and Wang disclose all the subject matters claimed in claim 13, except that the means for identifying includes at least one bus latch. Applicant in the background of invention discloses that at the rising or falling edge of each pulse, a device in the receiver referred to as a bus latch samples each stream (See page 1, lines 14-19). It would have been obvious to one of ordinary skill in the art at the time of invention to sample the received data by a bus latch at the receiver as suggested by Applicant's admitted prior art to sample the parallel data streams at the same time.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leila Malek whose telephone number is 571-272-8731. The examiner can normally be reached on 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Leila Malek
Examiner
Art Unit 2611

L.M

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER